## Features

- **32-kHz Voltage Regulated Oscillator**
- **1.1V to 2.2V Operating-voltage Range**
- **Integrated Capacitors for Digital Trimming**
- **Suitable for up to 12.5 pF Quartz**
- **Trimming Inputs Insenitive to Stray Capacitance**
- **Output Pulse Formers**
- **Mask Options for Motor Period and Pulse Width**
- **Low Resistance Output for Bipolar Stepping Motor**
- **Motor Fast-test Function**

## 1. Description

The e1467D is an integrated circuit in CMOS Silicon Gate Technology for analog clocks. It consists of a 32-kHz oscillator, frequency divider, output pulse formers, push-pull motor drivers and alarm output. Integrated capacitors are mask-selectable to accomodate the external quartz crystal. Additional capacitance can be selected through pad bonding to trimming the oscillator frequency.
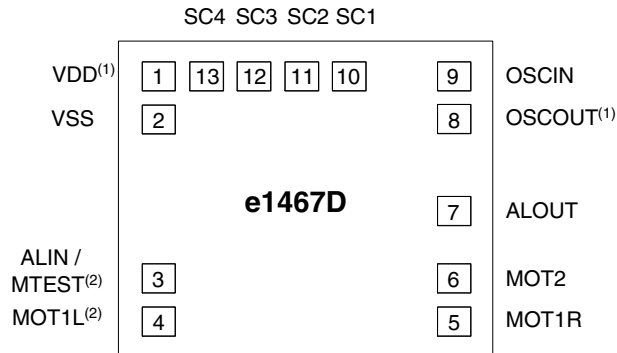
**32-kHz Clock CMOS IC with Digital Trimming and Alarm**

**e1467D**

## 2. Pad Configuration

**Figure 2-1.** Pad Configuration

SC4 SC3 SC2 SC1

```
VDD(1)    [1] [13] [12] [11] [10]   [9]  OSCIN
VSS       [2]                       [8]  OSCOUT(1)

                e1467D             [7]  ALOUT

ALIN /
MTEST(2)  [3]                      [6]  MOT2
MOT1L(2)  [4]                      [5]  MOT1R
```

(1) The pads VDD and OSCOUT are interchangeable per mask option

(2) The pads for ALIN/-MTEST and MOT1L are interchangeable per mask option

**Table 2-1.** Pin Description

| Name | Description |
|---|---|
| VDD | Positive supply voltage |
| VSS | Negative supply voltage |
| OSCIN | Oscillator input |
| OSCOUT | Oscillator output |
| MOT1/2 | Motor drive outputs |
| ALIN | Alarm input |
| ALOUT | Alarm output |
| SC1 ... SC4 | Oscillator trimming inputs |

## 3. Functional Descripion

### 3.1 Oscillator

An oscillator inverter with feedback resistor is provided to generate the 32768 Hz clock frequency. Values for the fixed capacitors at OSCIN and OSCOUT are mask-selectable (see note 3 of "Operating Characteristics"). Four control inputs, SC1 to SC4, enable the users to add integrated trimming capacitors to OSCIN and OSCOUT, providing 15 tuning steps.

A frequency variation of typically 4 ppm for each tuning step is obtained by bonding the capacitor pads to OSCIN. As none of these pads are bonded, the IC is in an untrimmed state. shows the trimming curve characteristic.

Note: For applications which utilize this integrated trimming feature, Atmel will determine optimum values for the integrated capacitors $C_{OSCIN}$ and $C_{OSCOUT}$.

### 3.2 Motor Drive Output

The e1467D contains two push-pull output buffers for driving bipolar stepping motors. During a motor pulse, the N-channel device of one buffer and the P-channel device of the other buffer will be activated. Both N-channel transistors are on and conducting between output pulses. The outputs are protected against inductive voltage spikes with diodes to both supply pins. The motor output period and pulse width are mask-programmable, as listed below:

Available motor periods ($T_M$): 125, 250, 500 ms and 2, 16s

Available maximum pulse widths ($t_M$): 15, 6, 23.4, 31.25, 46.9 ms

Available motor periods for motor test ($T_{MT}$): 250, 500 ms and 1s

Note: The following constraints for combination of motor period and pulse widths have to be considered: $T_M > 4 \times t_M$, $T_{MT} > 4 \times t_M$ or alternatively $T_M = 2 \times t_M$, $T_{MT} = 2 \times t_M$

### 3.3 Alarm Outputs

The alarm output driver consists of a push-pull stage for driving a speaker via an external bipolar transistor. The output is configured for NPN and PNP bipolar capability. The output is an alarm tone, modulated by a low frequency. Tone frequencies, modulation frequencies, and on/off times are selectable via the metal mask option.

### 3.4 Alarm Input

A debounced alarm input is provided. Alarm activation is connected either to $V_{DD}$ or $V_{SS}$ by a mask option.

### 3.5 Test Functions

For test purposes, the TEST pad is open. With a high resistance probe (R ≥ 10 MΩ, C ≥ 20 pF), a test frequency $f_{TEST}$ of 128 Hz can be measured at the ALIN/MTEST pad. Connecting ALIN/MTEST (for at least 32 ms) to the opposite polarity for alarm activation changes the motor period from the selected value to $T_{MT}$ (mask-selectable) while the pulse width remains unaffected. This feature can be used for testing the mechanical parts of the clock.

**Figure 3-1.** Functional Test
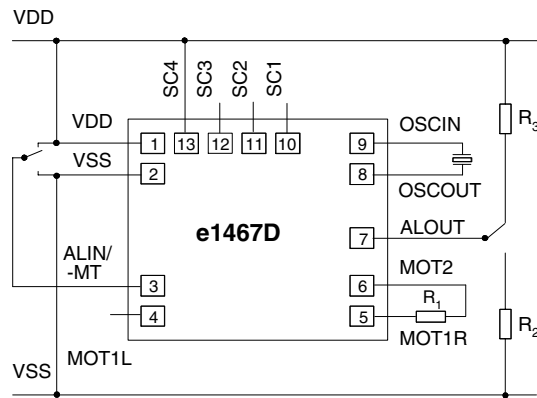


## 4. Test Crystal Specification

Oscillation frequency    $f_{OSC} = 32768$ Hz
Series resistance    $R_S = 30$ k$\Omega$
Static capacitance    $C_0 = 1.5$ pF
Dynamic capacitance    $C_1 = 3.0$ fF
Load capacitance    $C_L$ optionally 10 or 12.5 pF

## 5. Absolute Maximum Ratings

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device.
All inputs and outputs on Atmel's circuits are protected against electrostatic discharges. However, precautions to minimize the build-up of electrostatic charges during handling are recommended.
The circuit is protected against supply voltage reversal for typically 5 minutes.

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | $V_{SS}$ | –0.3 to 5 V | V |
| Input voltage range, all inputs | $V_{IN}$ | $(V_{SS} - 0.3V) \leq V_{IN} \leq (V_{DD} + 0.3V)$ | V |
| Output short circuit duration | | indefinite | |
| Power dissipation (DIL package) | $P_{tot}$ | 125 | mW |
| Operating ambient temperature range | $T_{amb}$ | –20 to +70 | °C |
| Storage temperature range | $T_{stg}$ | –40 to +125 | °C |
| Lead temperature during soldering at 2 mm distance, 10 s | $T_{sld}$ | 260 | °C |

# 6. Operating Characteristics

$V_{SS} = $ 0V, $V_{DD} = $ 1.5V, $T_{amb} = $ +25°C, unless otherwise specified.
All voltage levels are measured with reference to $V_{SS}$. Test crystal as specified below.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating voltage | | $V_{DD}$ | 1.1 | 1.5 | 2.2 | V |
| Operating temperature | | $T_{amb}$ | −20 | | +70 | °C |
| Operating current | $R_1 = \infty^{(2)}$ | $I_{DD}$ | | 1 | 3 | μA |
| **Motor Drive Output** | | | | | | |
| Motor output current | $V_{DD} = $ 1.2V, $R_1 = $ 200 Ω | $I_M$ | ±4.3 | | | mA |
| Motor period | | $T_M$ | See option list | | | s |
| Motor period during motor test | | $T_{MT}$ | See option list | | | ms |
| Motor pulse width | | $t_M$ | See option list | | | ms |
| **Oscillator** | | | | | | |
| Start-up voltage | Within 2s | $V_{START}$ | 1.2 | | 2.2 | V |
| Frequency stability | $\Delta V_{DD} = $ 100 mV, $V_{DD} = $ 1.1 to 2.2V | $\Delta f/f$ | | 0.1 | 0.2 | ppm |
| Integrated input capacitance | (3) | $C_{OSCIN}$ | See option list | | | pF |
| Integrated output capacitance | | $C_{OSCOUT}$ | See option list | | | pF |
| Input current SC1 to SC4 | $V_{IN} = $ 0.2V<br>$V_{IN} = V_{DD}^{(5)}$ | $I_{SCINL}$<br>$I_{SCINH}$ | 1<br>0.05 | 5<br>0.15 | 25<br>0.5 | μA<br>μA |
| **Alarm/Output** | | | | | | |
| Output current for driving npn transistor | $V_{DD} = $ 1.2V | | | | | |
| N-channel | $R_3 = $ 100 kΩ | $I_{ANn}$ | 1 | 3 | 10 | μA |
| P-channel | $R_2 = $ 1 kΩ$^{(2)(4)}$ | $I_{ANp}$ | −0.5 | −1 | | mA |
| Output current for driving pnp-transistor | $V_{DD} = $ 1.2V | | | | | |
| N-channel | $R_3 = $ 1 kΩ | $I_{APn}$ | 0.5 | 1 | | mA |
| P-channel | $R_2 = $ 100 kΩ$^{(2)(4)}$ | $I_{APp}$ | −1 | −2 | −10 | μA |
| **Alarm Options** | | | | | | |
| Tone frequency | | $f_A$ | See option list | | | Hz |
| Modulation frequency | | $f_{MOD}$ | See option list | | | Hz |
| On/off time | | $t_{ON}/t_{OFF}$ | See option list | | | s |
| **Alarm Input/Motor Test** | | | | | | |
| Input current | ALIN = $V_{DD}$, peak current | $I_{AINH}$ | 0.6 | 3 | 10 | μA |
| Input current | ALIN = $V_{SS}$, peak current | $I_{AINL}$ | −0.6 | −3 | −10 | μA |
| Input debounce delay | | $t_{AIN}$ | 23.4 | | 31.2 | ms |

Notes: 1. Typical parameters represent the statistical mean values

2. See test circuit

3. Values can be selected in 1 pF steps. A total capacitance ($C_{OSCIN} + C_{OSCOUT}$) of 38 pF is available

4. NPN or PNP driving transistors defined by mask options

5. $I_{SCINH}$ is the peak current of a pulsed current with a duty cycle of 1:63. Average current is always smaller than 10 nA

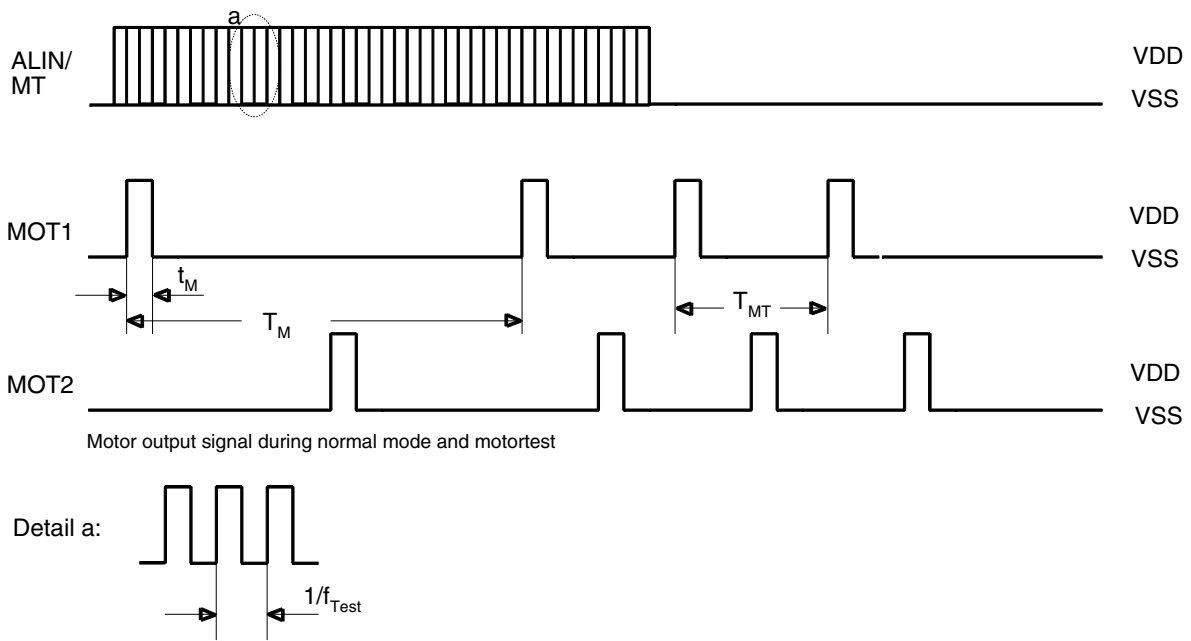**Figure 6-1.** Motor Output Signal During Normal Operation and During Motor Test

Motor output signal during normal mode and motortest

Detail a:

$1/f_{Test}$

**Figure 6-2.** Alarm Operation



Signal on alarm input and alarm output during alarm activation

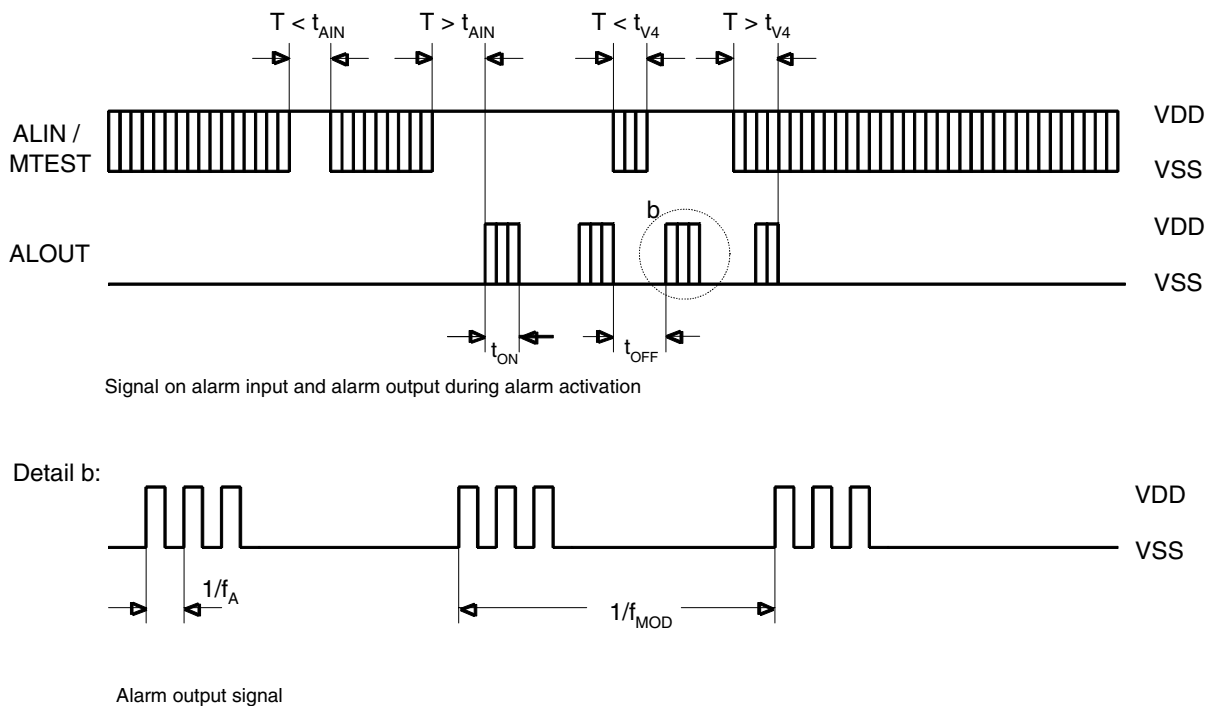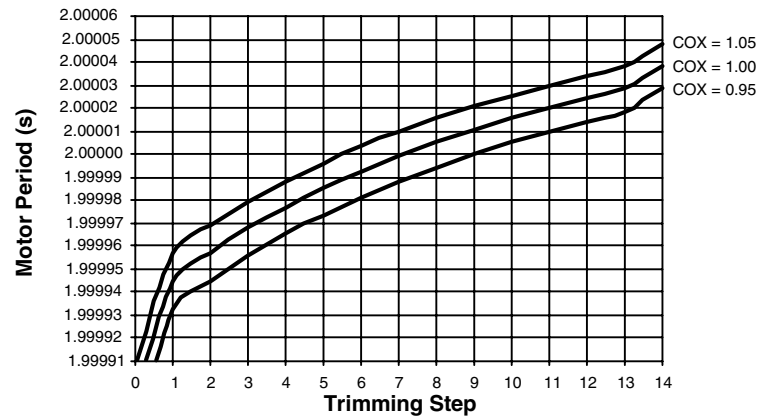Detail b:

$1/f_A$

$1/f_{MOD}$

Alarm output signal

**Figure 6-3.** Typical Trimming Curve Characteristic for $T_M$ of 2s



$C_{OX}$ means frequency deviation due to production process variations.

Trimming inputs SC1 ... SC4 are binary weighted, i.e.,
SC1 ... SC4 = 0 corresponds to trimming step 0
SC1 ... SC4 = 1 corresponds to trimming step 15

LSB = SC1

## 7. Ordering Information

**Table 7-1.** Option List e1467Dx

| Option | Motor | | | Alarm | | | | | Load Cap. | Integrated Capacitance | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| x | Cycle $(T_M)$ s | Pulse $(t_M)$ ms | Test $(T_{MT})$ ms | Frequency Hz | Modulation Frequency Hz | On/off Time s | Driver Type | Activation Polarity | pF | $C_{OSCIN}$[1] pF | $C_{OSCOUT}$[1] pF |
| B | 2 | 23.4 | 250 | 2048 | 8 | 0.5/0.5 | NPN | $V_{SS}$ | 10 | 17 | 12 |
| D | 2 | 31.25 | 250 | 2048 | 8 | 0.5/0.5 | NPN | $V_{DD}$ | 10 | 17 | 12 |
| V2 | 0.5 | 23.4 | 250 | 2048 | 8 | 0.5/0.5 | NPN | $V_{SS}$ | 12.5 | 20 | 16 |
| E2 | 2 | 46.9 | 250 | 2048 | 8 | 1/3 | NPN | $V_{SS}$ | 12.5 | 20 | 16 |

Note: 1. On-chip stray capacitance included

| Option | Pad Designation | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Pad 1 | Pad 2 | Pad 3 | Pad 4 | Pad 5 | Pad 6 | Pad 7 | Pad 8 | Pad 9 | Pad 10 | Pad 11 | Pad 12 | Pad 13 |
| B | OSCIN | $V_{DD}$ | ALOUT | MOT2 | MOT1 | MOT1 | ALIN/MTEST | $V_{SS}$ | OSCOUT | SC4 | SC3 | SC2 | SC1 |
| D | OSCIN | OSCOUT | ALOUT | MOT2 | MOT1 | MOT1 | ALIN/MTEST | $V_{SS}$ | $V_{DD}$ | SC4 | SC3 | SC2 | SC1 |
| V2 | OSCIN | $V_{DD}$ | ALOUT | MOT2 | MOT1 | MOT1 | ALIN/MTEST | $V_{SS}$ | OSCOUT | SC4 | SC3 | SC2 | SC1 |
| E2 | OSCIN | OSCOUT | ALOUT | MOT2 | MOT1 | ALIN/TEST | MOT1 | $V_{SS}$ | $V_{DD}$ | SC4 | SC3 | SC2 | SC1 |

**Table 7-2.** Package List

| Extended Type Number | Package | Remarks |
|---|---|---|
| e1467Dx-DIT | Die-in-tray | - |

## 8. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|---|---|
| 4733B-CLOCK-08/05 | • Put datasheet in a new template<br>• Table 7-1 heading "Option List e1467Dx", column Option changed on page 8<br>• Table 7-2 extended type number changed on page 8 changed<br>• Page 8: Table 7-2: Package List added |

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